What is claimed is:

1. A method for predicting values in a processor having a plurality of prediction modes, comprising:

receiving an instruction at a first table;

generating a valid signal from said first table;

providing a prediction mode for said instruction;

determining a hit in a second table according to a function of said instruction and said first table; and

predicting a predicted value according to said hit and said prediction mode.

2. The method of claim 1, wherein said predicting includes selecting said predicted value from said first table.

3. The method of claim 1, wherein said predicting includes selecting said predicted value from said second table.

4. The method of claim 1, wherein said predicting includes selecting said predicted value from said first table or said second table according said hit in said second table.

5. The method of claim 1, wherein said generating includes matching a first table tag with said instruction.

6. The method of claim 5, wherein said generating further includes accessing an information field in said first table correlating to said first table tag.

7. The method of claim 1, further comprising placing said prediction mode in a shift mode.

8. The method of claim 1, further comprising placing said prediction mode in a count mode.

9. The method of claim 1, further comprising placing said prediction mode in a stride mode.

10. The method of claim 1, wherein said providing includes providing said prediction mode from said first table.

11. The method of claim 1, further comprising transitioning to said prediction mode from a previous prediction mode.

12. The method of claim 1, further comprising indexing said second table according to said function and a subset of said instruction.

13. A multi-mode predictor in a processor, comprising:

a first table indexed by an instruction pointer and having table entries that includes a mode field and a information field;

a second table indexed by a function of said instruction pointer and said first table; and a hit condition in said second table that correlates to a predicted value of a prediction mode.

14. The multi-mode predictor of claim 13, wherein said prediction mode is a shift mode.

15. The multi-mode predictor of claim 13, wherein said prediction mode is a count mode.

16. The multi-mode predictor of claim 13, wherein said prediction mode is a stride mode.

17. The multi-mode predictor of claim 13, wherein said first table provides said predicted value.

18. The multi-mode predictor of claim 13, wherein said second table provides said predicted value.

19. A processor, comprising:

a multi-mode predictor comprising a first table and a second table, wherein said first table includes a plurality of entry fields and said second table includes a plurality of entry fields, and having a plurality of prediction modes;

a set of instructions that index said first table to provide a signal; and

a set of predicted values for said set of instructions, said set of predicted values stored in said first table and said second table.

20. The processor of claim 19, wherein said multi-mode predictor further comprises a function that indexes said second table according to said set of instructions and said first table entry fields.

21. The processor of claim 19, wherein said set of predicted values includes a first set of predicted values stored in said first table, and a second set of predicted values stored in said second table.

22. The processor of claim 21, further comprising a hit condition in said second table that accesses said second set of predicted values.

23. The processor of claim 21, further comprising a miss condition in said second table that accesses said first set of predicted values.

24. A multimode predictor, comprising:

a first table, indexed by an instruction pointer and having first table entries, each having a mode field and a first prediction result field;

a function unit having an input for instruction pointer data and coupled to said first prediction result fields of the first table entries, and having an output for a calculated pointer;

a second table indexed by the calculated pointer and having second table entries having second prediction result fields; and

a selector, having a control input coupled to the mode fields and data inputs coupled to the first and second prediction result fields.

25. The predictor of claim 24, wherein the first prediction result fields comprise a stride sub-field and a last value sub-field.

26. The predictor of claim 24, wherein the first table generates a signal indicating whether the instruction pointer hit the first table.